

ABSTRACT OF THE INVENTION

A fast pipelined adder/subtractor using increment/decrement functions with reduced register utilization. Embodiments of the present invention replace
5 double width registers with incrementor elements, pipelined single width registers, and pipelined carry bits. This is made possible by positioning the adder elements at the first pipestage in each of the pipelines. Single width registers are used to hold the results of the initial add/subtract operation. Single bit registers pipeline the carry bits from the adders and incrementors to the next
10 stage. The incrementor collects the sum from one of the adder elements, the pipelined carry bit from that adder element, and the carry bit from a previous stage adder and combines them to produce a new result and carry. This new result is passed along the pipeline to the output bus of the circuit. In this fashion, no double width busses or registers are required in between individual
15 pipestages of the pipelines.